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(54) Oscillator circuit having oscillation frequency independent from the supply voltage valu

(57) The oscillating circuit in accordance with the present invention comprises a capacitor C, a charge circuitry CCA and a control circuitry CCO. The charge circuitry CCA includes a first GEN1 and a second GEN2 current generators having respectively a first and a second current values and opposite directions and switching means SW1,SW2 designed to couple alternatively the generators GEN1,GEN2 to the capacitor C. The control circuitry CCO has a voltage input coupled to the capacitor C and an output coupled to control inputs of the switching means SW1,SW2 and includes a comparator with hysteresis having a lower threshold and an upper threshold.

If for the difference between the upper threshold and the lower threshold a value is chosen essentially proportional to the ratio of the product to the sum of the two current values the oscillation frequency and the duty cycle depend neither on the supply voltage nor the temperature nor the process.

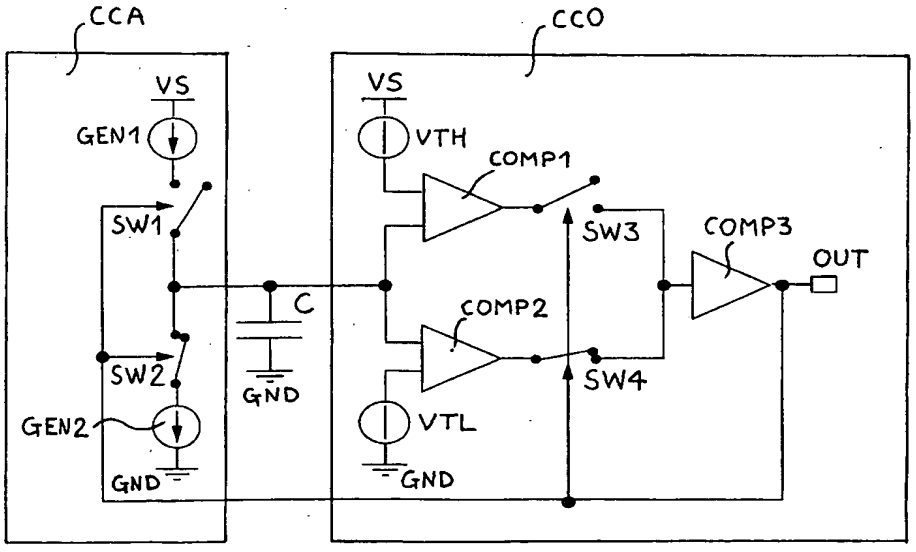

Fig.2

EP 0 735 677 A1

Description

The present invention relates to a method for generating an oscillating electric signal and associated oscillating circuit.

Oscillators are widely used in analog and digital circuits. They can be employed in a large number of applications, for example to drive a voltage multiplier, generate a clock frequency or create a programmable delay. Usually a good oscillator must be able to operate at high switching frequency, have an oscillation frequency independent of the supply voltage and variations in process and temperature, have a duty cycle definable in accordance with a constant ratio and have low electromagnetic interference (EMI), i.e. primarily voltage edges with controlled and not too high slope.

A very simple oscillating circuit can be achieved by connecting in a loop two inverters, one resistor and one capacitor and generating an oscillating electric signal having an essentially square shape. Naturally this simple circuit does not meet the above mentioned requisites and in particular the oscillation frequency depends both on the supply voltage and the switching threshold of the inverters and hence on the temperature and the process.

From the article by S.Hobrecht, "An Intelligent BiCMOS/DMOS Quad 1-A High-Side Switch", IEEE Journal of Solid-State Circuits, Vol.25, No.6, December 1990 and in particular FIG. 4 and the corresponding description on page 1397, a more sophisticated circuit is known and shown in the annexed FIG. 1.

It comprises a first inverter INV1, a second inverter INV2 and two symmetrical and analogous sections, the first of which comprises a first capacitor C1 having a first and a second terminals, a first current generator GEN1 having an input terminal and an output terminal, a first transistor SW1 of the p-channel MOS type and a first controlled switch SW3. Analogously the second section comprises a second capacitor C2 having a first and a second terminal, a second current generator GEN2 having an input terminal and an output terminal, a second transistor SW2 of n-channel MOS type and a second controlled switch SW4.

The circuit is powered by means of connection to a ground terminal GND and a power supply terminal VS. The output terminal OUT is connected to the output of the inverter INV2.

If the two capacitors have the same capacitance Co and the generators GEN1 and GEN2 have the same current Io, oscillation frequency will be:

$$f_0 = \frac{I_0}{VS \cdot C_0}$$

and hence depends on the supply voltage; the duty cycle depends on the switching threshold of the inverters (and hence on the temperature and process); and in addition, despite the fact that the voltages across the capacitors have a triangular shape which should involve a low electromagnetic interference, this interference is high enough that the falling edges have a rather high slope (the shape is more correctly termed "saw tooth") as shown in FIG. 4 of this article.

Of course this circuit is very sensitive to the symmetry of its components.

The purpose of the present invention is to supply a method of generating an oscillating electric signal and an associated oscillating circuit overcoming the shortcomings of the prior art.

The purpose is achieved through the method having the functions set forth in claim 1 and through the circuit having the characteristics set forth in claim 8. Other advantageous aspects of the present invention are set forth in the dependent claims.

By using a single capacitor charged and discharged by two current generators having a first and a second value and causing the voltage at its ends to have a truly triangular shape and an amplitude corresponding essentially to the ratio of the product to the sum of the two values, the oscillation frequency and duty cycle depend neither on the supply voltage nor on temperature nor process.

In accordance with another aspect the present invention relates also to an integrated circuit in which the oscillating circuit finds advantageous application.

The present invention is clarified by the description given below examined together with the annexed drawings in which:

FIG. 1 shows a simplified circuit diagram of an oscillating circuit in accordance with the prior art,

FIG. 2 shows a simplified circuit diagram of a possible oscillating circuit in accordance with the present invention, and

FIG. 3 shows a circuit diagram of a possible embodiment of the circuit of FIG. 2.

With reference to FIG. 2 the oscillating circuit comprises a capacitor C, a charge circuitry CCA and a control circuitry CCO.

The charge circuitry CCA comprises a first current generator GEN1 and a second current generator GEN2 having respectively a first and a second current value and opposite directions (meaning that one is capable of supplying current at the output of the circuitry CCA and the other of absorbing it) and switching means corresponding to a first switch SW1 and a second switch SW2 designed to alternatively couple the generators GEN1 and GEN2 to the capacitor C.

The control circuitry CCO has a voltage input coupled to the capacitor C and has an output coupled to control inputs of the switches SW1, SW2 and includes a comparator with hysteresis having a lower threshold and an upper threshold.

The difference between the upper threshold and the lower threshold must be chosen equal to a value

essentially proportional to the ratio of the product to the sum of the two current values.

The circuit is powered in the example of FIG. 2 by means of connection to a ground terminal GND and to a power supply terminal VS. It is also possible to use positive and negative power supply sources.

There are various points of this circuit at which is present an oscillating signal which could be used as an output, for example the voltage across the capacitor C. It is advantageous to connect the output OUT of the circuit to the output of the comparator with hysteresis, i.e. to the output of the circuitry CCO and indeed this will have a shape essentially corresponding to a square wave and in general will not necessitate bufferization since the output of an impedance comparator is relatively low.

If the two current values are essentially equal implementation of the circuit is much simpler.

If the generators GEN1, GEN2 are mutually interlocked operation of the circuit is steadier and independent of process and temperature changes.

In FIG. 2 the circuitry CCO has one input and one output and includes two comparators COMP1 and COMP2, an inverter COMP3, two controlled switches SW3, SW4, a first voltage generator VTH and a second voltage generator VTL.

The generator VTH is connected to the power supply terminal VS in such a manner that a first reference potential thus generated corresponds to the upper threshold (which is lower than the supply voltage). The generator VTL is connected to the ground terminal GND in such a manner that a second reference potential thus generated corresponds to the lower threshold (which is higher than zero).

The input of the circuitry CCO is connected to a first input of the comparator COMP1 while the first reference potential is supplied to a second input of the comparator COMP1. The input of the circuitry CCO is connected to a first input of the comparator COMP2 while the second reference potential is supplied to a second input of the comparator COMP2. The comparators COMP1 and COMP2 are such as to supply at output a "high" logical signal when the potential at their first input is higher than the potential at their second input and vice versa.

The input of the inverter COMP3 is connected to the outputs of the comparators COMP1 and COMP2 respectively through the switches SW3 and SW4. The latter have control terminals connected together and are such that when one of the two is open the other is closed and vice versa. The output of the inverter COMP3 is connected to the control terminals of the switches SW3, SW4. When the output is in "high" logic state the switch SW3 is closed and the switch SW4 is open and hence the output of the comparator COMP1 is connected to the input of the inverter COMP3 and when the output is in "low" logic state the switch SW3 is open and the switch SW4 is closed hence the output of the comparator COMP2 is connected to the input of the inverter COMP3. Furthermore the output of the comparator COMP3 is connected to the output of the circuitry CCO.

It is natural that both the comparators and the inverter have a small intrinsic delay.

The above described circuit possess essentially two operational conditions, i.e. the first operational condition corresponds to the injection into the capacitor C of the current supplied by the generator GEN1 and the second operational condition corresponds to the extraction from the capacitor C of the current absorbed by the generator GEN2.

The circuitry CCO is designed to activate alternatively the first or second operational condition depending on whether the voltage across the capacitor C has passed the lower threshold while decreasing or the upper threshold while increasing respectively.

It is advantageous that the switches SW1, SW2 be designed to couple alternatively the first generator GEN1 and the second generator GEN2 at constant potential nodes respectively through a first and a second paths. Indeed, in this manner the two generators are never turned off and back on since these are in general slow operations designed to originate transistors which would have negative repercussions on circuit performance.

The oscillation frequency of the circuit of FIG. 2 is given by

$$f=\frac{1}{\frac{DV \cdot C}{I1}+\frac{DV \cdot C}{I2}}=\frac{I1 \cdot I2}{DV \cdot C \cdot (I1+I2)}$$

where DV indicates the voltage range across the capacitor C, C the capacitance of the capacitor, and I1 and I2 the current respectively of the generator GEN1 and generator GEN2.

From this formula it is clear that if DV is essentially proportional to the ratio of the product to the sum of the two values I1 and I2 the frequency depends only on the value C and the proportionality factor.

The circuit of FIG. 3 is a circuit diagram of a possible embodiment of the circuit of FIG. 2.

The current generators GEN1 and GEN2 are made up respectively of the p-channel transistors P2 and n-channel transistors N2. Their source terminals are respectively connected to the power supply terminal VS and to the ground terminal GND. The drain terminals constitute the respective outputs. The control terminals are connected together through an electrical network which interlocks them mutually.

This network includes a p-channel transistor P1, an n-channel transistor N1 and a resistor R. The transistor P1 is diode-connected and has its source terminal connected to the terminal VS and its control terminal connected to the control terminal of the transistor P2. The transistor N1 is diode-connected and has its source terminal connected to the terminal GND and its control terminal connected to the control terminal of the transistor

N2. The resistor R is connected between the drain terminals of the transistors P1 and N1.

If the area ratios between the transistors P1 and P2 and between N1 and N2 arethe same and equal to 1:1 the currents I1 and I2 generated by the two generators GEN1 and GEN2 will have the same value equal to:

$$I=\frac{VS-VGS(P2)-VGS(N2)-Vgnd}{R}$$

where it is necessary to allow for the fact that the VGS of the transistors P2 and N2 depends on the bias current which in this case corresponds to I since the pairs P1, P2 and N1, N2 behave as current mirrors.

The switch SW1 consists of two p-channel transistors S1 and S3 having their source terminals connected to the drain terminal of the transistor P2. The switch SW2 consists of two n-channel transistors S2 and S4 having their source terminals connected to the drain terminal of the transistor N2. The drain terminals of the transistors S1 and S2 are connected together to a first terminal of the capacitor C. The drain terminals of the transistors S3 and S4 are connected together. The control terminals of the transistors S1 and S2 are connected together. The control terminals of the transistors S3 and S4 are connected together. The second terminal of the capacitor C is connected to the ground terminal GND (it could also be connected to another reference potential).

The group formed by the comparator COMP1 and the generator VTH is implemented by means of a p-channel transistor P3 and the switch SW3 is implemented by means of a p-channel transistor S5. The source terminal of the transistor P3 is connected to the terminal VS and the source terminal of the transistor S5 is connected to the drain terminal of the transistor P3.

The group made up of the comparator COMP2 and the generator VTL is implemented by means of an n-channel transistor N3 and the switch SW4 is implemented by means of an n-channel transistor S6. The source terminal of the transistor N3 is connected to the terminal GND and the source terminal of the transistor S6 is connected to the drain terminal of the transistor N3.

The control terminals of the transistors N3 and P3 are connected together to the first terminal of the capacitor C. The control terminals of the transistors S5 and S6 are connected together.

The drain terminals of the transistors S5 and S6 are connected together either to the drain terminals of the transistors S3 and S4 or to the input of a first inverter INV1 whose output is connected to the input of a second inverter INV2.

The outputs of the inverters INV1 and INV2 correspond essentially to the output of the circuitry CCO. In the example of FIG. 3 the output OUT of the oscillator has been connected to the output of the inverter INV2.

The output of the inverter INV1 goes to drive the control terminals of the transistors S1, S2, S5, S6. The output of the inverter INV2 goes to drive the control terminals of the transistors S3 and S4.

The transistors N3 and P3 operate as comparators and specifically compare the voltage across the capacitor C respectively with the threshold voltage of the transistor N3 referred to ground (lower threshold) and the difference between the supply voltage and the threshold voltage of the transistor P3 (upper threshold). These threshold voltages mentioned are not however the intrinsic ones of the transistors but are the voltages VGS of those transistors at the bias current, i.e. VGS(N3) and VGS(P3).

If the transistors P2 and P3 are essentially equal and the transistors N2 and N3 are essentially equal, then VGS(N2)=VGS(N3) and VGS(P2)=VGS(P3), current being equal, and the oscillation frequency will be equal to 1/RC independent of process temperature and supply voltage.

The duty cycle of the oscillation is strictly 50% and depends only on the area ratios of the transistors N1, N2, N3, P1, P2, P3.

The electromagnetic interference is reduced to the minimum because the voltage across the capacitor C has an "actually" triangular shape and furthermore the edges of the triangle are slightly rounded.

The circuit of FIG. 3 achieves equality of the VGS in a particularly advantageous manner.

When the transistor S2 conducts, the current generated by the transistor N2 discharges the capacitor C and at the same time the transistors S1 and S4 do not conduct while the transistor S3 conducts and causes the current generated by the transistor P2 to run through the main conduction paths of the transistors N3 and S6 which are thus biased.

When the transistor S1 conducts, the current generated by the transistor P2 charges the capacitor C and at the same time the transistors S2 and S3 do not conduct while the transistor S4 conducts and causes the current generated by the transistor N2 to run through the main conduction paths of the transistors P3 and S5 which are thus biased.

If the transistors P2 and P3 are essentially equal and the transistors N2 and N3 are essentially equal, all four of these transistors are traversed by the same bias current and thus have the same VGS. This is achieved by an extremely simple circuitry and furthermore energy dispersal is minimized since the current of the generator not used at a predetermined time for charge/discharge of the capacitor C is used for biasing the transistor which must make the comparison with the threshold involved.

The comparison for example with the lower threshold takes place in the following manner. Assuming that the capacitor is found at a voltage corresponding for example to one-half of the supply voltage, the transistor N2 extracts its current through the transistor S2 from the capacitor C and then the voltage at its ends falls and simultaneously the transistor P2 keeps the transistor N3 biased through the transistors S3 and S6. As the volt-

age VGS of the transistor N3 falls its voltage VDS rises slowly since the current ID remains steady and this continues until saturation conditions of the transistor N3 are neared. Once saturation conditions are reached a minimal decrease in the VGS involves a high increase in the VDS of the transistor N3 which leads to switching of the inverter INV1 first and then the inverter INV2.

It is not extremely simple to determine with extreme accuracy the value of the VGS for switching of the transistors N3 and P3 nor therefore of the lower and upper thresholds because these transistors operate at the border between the saturation region and the linear region and hence the models and formulas normally used in the two regions are applicable only in a first approximation. But this is not extremely important for the purposes of operation of the circuit.

The present invention finds advantageous application in integrated circuits of the type which can be powered at low voltage (for example 3V). In these circuits it is often necessary to generate higher supply voltages. This is done by means of voltage boosting circuits with charge pump.

These booster circuits require an oscillating electric signal at the input.

In the above mentioned article of S. Hobrecht there is shown for example in FIG. 5 and described on pages 1397 and 1398 a voltage tripling circuit necessary for driving the control terminal of an MOS power transistor.

As mentioned above the present invention finds application in integrated circuits even for other purposes such as for example the generation of clock signals or programmable delays.

Claims

1. Method for generating an oscillating electric signal through an electric circuit comprising a capacitor (C), a charge circuitry (CCA) and a control circuitry (CCO) and in which said charge circuitry (CCA) possesses at least one first and one second operational conditions and said first operational condition corresponds to the injection in said capacitor (C) of a current having a first value and said second operational condition corresponds to the extraction from said capacitor (C) of a current having a second value and in which said control circuitry (CCO) is designed to activate alternatively said first or said second operational condition depending on whether the voltage across said capacitor (C) has passed a lower threshold while decreasing or an upper threshold while increasing respectively with the difference between said upper threshold and said lower threshold having a value proportional essentially to the ratio of the product of said first and said second values to the sum of said first and second values so that said oscillating electric signal corresponds to the voltage across said capacitor (C).

2. Method in accordance with claim 1 characterized in that said oscillating electric signal corresponds to a voltage signal obtained essentially by squaring the voltage across said capacitor (C).

3. Method in accordance with claim 1 characterized in that said first and second values are essentially equal.

4. Method in accordance with claim 1 characterized in that said first and second operational conditions are achieved by connecting to said capacitor (C) respectively a first (GEN1) and a second (GEN2) current generators mutually interlocked (P1,R,N1).

5. Method in accordance with claim 4 characterized in that in said first operational condition said first generator (GEN1) is coupled to said capacitor (C) and said second generator (GEN2) is coupled through a second path to a constant potential node and in said second operational condition said second generator (GEN2) is coupled to said capacitor (C) and said first generator (GEN1) is coupled through a first path to a constant potential node.

6. Method in accordance with claim 4 or 5 characterized in that for said first (GEN1) and second (GEN2) generators are used respectively a first (P2) and a second (N2) threshold devices as output devices in such a manner that said first and second values depend on the sum of the thresholds of said first (P2) and second (N2) devices and in that for said control circuitry (CCO) are used a third (P3) and a fourth (N3) threshold devices respectively and essentially equal to said first (P2) and second (N2) threshold devices in such a manner that said upper threshold depends on the threshold of said third (P3) device and said lower threshold depends on the threshold of said fourth (N3) device.

7. Method in accordance with claims 5 and 6 characterized in that said first path is such as to include the main conduction path of said fourth device (N3) and in that said second path is such as to include the main conduction path of said third device (P3).

8. Oscillating circuit comprising a capacitor (C), a charge circuitry (CCA) and a control circuitry (CCO) and characterized in that said charge circuitry (CCA) includes a first (GEN1) and a second (GEN2) current generators having respectively a first and a second current values and opposite directions and switching means (SW1,SW2) designed to couple alternatively said generators (GEN1,GEN2) to said capacitor (C) and in that said control circuitry (CCO) has a voltage input coupled to said capacitor (C) and an output coupled to control inputs of said switching means (SW1,SW2) and includes a comparator with hysteresis having a

lower threshold and an upper threshold and in that the difference between said upper threshold and said lower threshold has a value proportional essentially to the ratio of the product of said first and second values to the sum of said first and second values.

9. Circuit in accordance with claim 8 and characterized in that the output of said oscillator is coupled to the output of said comparator with hysteresis.

10. Circuit in accordance with claim 8 and characterized in that said first and second values are essentially equal.

11. Circuit in accordance with claim 8 and characterized in that said generators (GEN1,GEN2) are mutually interlocked by means of an electrical network (P1,R,N1).

12. Circuit in accordance with claim 8 and characterized in that said switching means (SW1,SW2) are designed to couple alternatively said first (GEN1) and second (GEN2) generators to constant potential nodes respectively through a first and a second path.

13. Circuit in accordance with claim 8 and characterized in that said first (GEN1) and second (GEN2) generators comprise respectively a first (P2) and a second (N2) threshold devices as output devices and in that said first and second values depend on the sum of the thresholds of said first (P2) and second (N2) devices and in that said control circuitry (CCO) includes a third (P3) and fourth (N3) threshold devices respectively and essentially equal to said first (P2) and second (N2) devices and in that said upper threshold depends on the threshold of said third (P3) device and said lower threshold depends on the threshold of said fourth (N3) device.

14. Circuit in accordance with claims 12 and 13 and characterized in that said first path includes the main conduction path of said fourth device (N3) and in that said second path includes the main conduction path of said third device (P3).

15. Integrated circuit of the type which can be powered with low voltage and comprising a voltage boosting circuit with charge pump and an oscillating circuit in accordance with one of claims 8 to 14 connected to the input of said booster circuit.

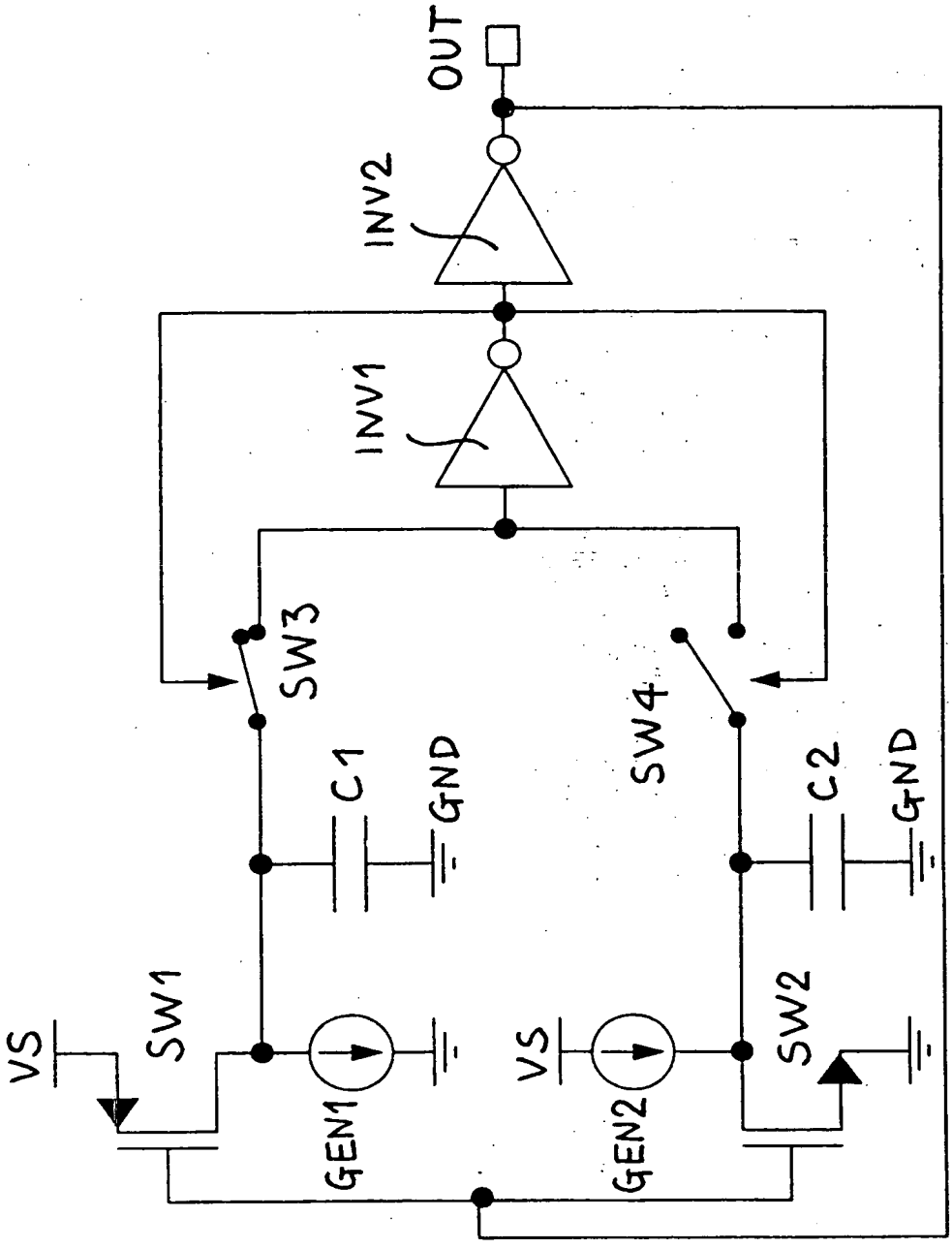

Fig.1

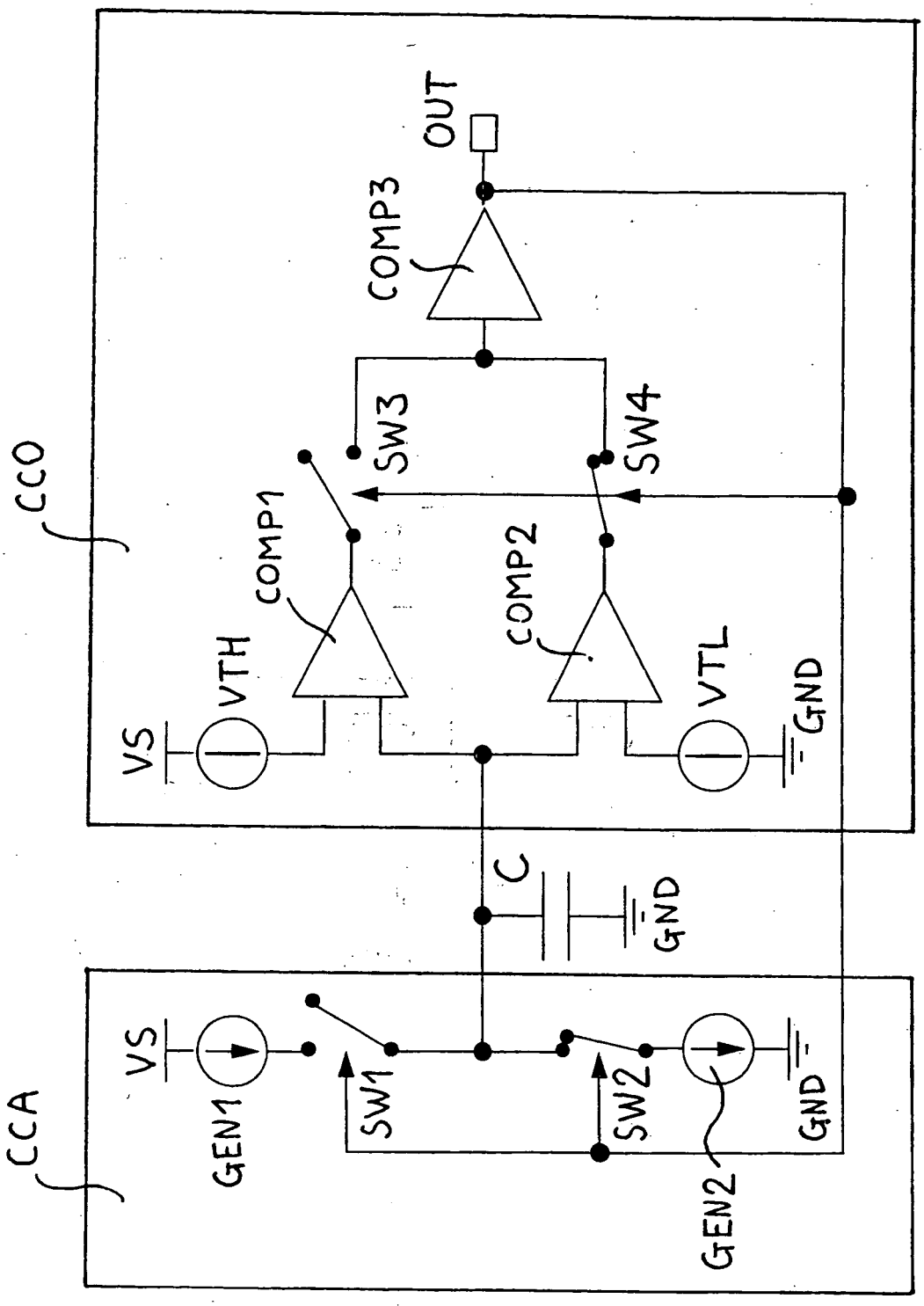
CCO
OUT
COMP3
SW3
SW4
COMP1
COMP2
VS
VTH
VTL
GND
C
GND
CCA
VS
GEN1
SW1
SW2
GND
GEN2

Fig.2

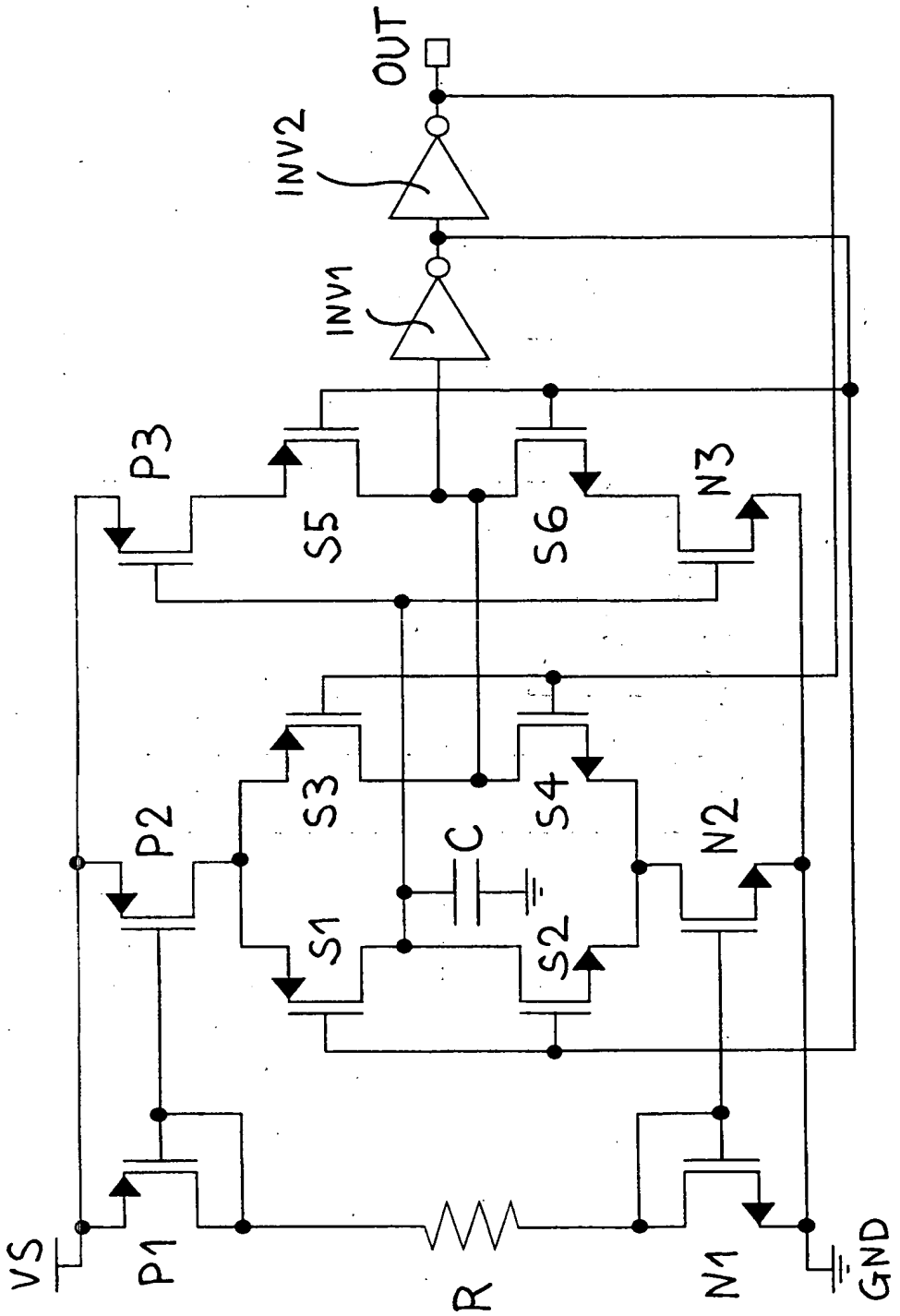

Fig. 3

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EUROPEAN SEARCH REPORT

Application Number
EP 95 83 0123

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X Y	US-A-4 594 565 (BARRERAS) * column 3, line 42 - column 8, line 66 * * figures 3-5 *	1-4,8-11 5,12,15	H03K3/011 H03K3/0231
Y	PATENT ABSTRACTS OF JAPAN vol. 9 no. 19 (E-292) [1742] ,25 January 1985 & JP-A-59 165516 (YOKOGAWA HOKUSHIN DENKI K.K.) 18 September 1984, * abstract *	5,12	
D,Y	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 25, no. 6, December 1990 NEW YORK US, pages 1395-1402, XP 000176568 HOBRECHT 'An Intelligent BiCMOS/DMOS Quad 1-A High-Side Switch' * figures 4,5 *	15	
A	US-A-5 250 914 (KONDO) * column 4, line 7 - column 8, line 58 * * figures 6-9 *	1-14	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H03K
A	EP-A-0 231 872 (SIEMENS AKTIENGESELLSCHAFT BERLIN UND MÜNCHEN) * column 3, line 1 - line 16 * * figure 3 *	5-7, 12-14	
A	US-A-4 983 931 (NAKANO) * the whole document *	1-14	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	22 August 1995	Jepsen, J

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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